A Double Lightly Doped Drain (D-LDD) Structure H-MESFET for MMIC Applications

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***Abstract*— This paper proposes a new double lightly doped drain (D-LDD) structure for InGaP/InGaAs heterostructure MESFET's (H-MESFET's). A D-LDD H-MESFET has three kinds of low-resistant layers in the drain region, while a conventional LDD H-MESFET has two layers. This structure improves maximum stable gain (MSG) accompanied by R_d reduction with minimized gate–breakdown–voltage degradation and $C_{\rm gd}$ increase. A heuristic model is proposed to predict $V_{\rm bgd}$ from sheet resistance of implanted layers, and its validity is confirmed with experimental data. This model successfully predicted the tradeoff relation between $V_{\rm bgd}$ and parasitic resistance, and it has enough generality so that it can be applied to usual ion-implanted GaAs MESFET's. Consequently, a typical MSG at 50 GHz exhibits 8.9 dB in a MESFET and 7.7 dB $S21$ in an one-stage amplifier. The high-frequency circuit operation proves that this technology is one of the most promising for monolithic-microwave integrated-circuit (MMIC) applications.**

***Index Terms*—GaAs, microwave amplifier, MESFET, MMIC.**

I. Introduction

IN THE coming multimedia age, ultra-broad-band wireless-access systems will become necessary for dealing with large amounts of information. In order to realize these systems, millimeter-wave and monolithic microwave integrated circuits (MMIC's) will be indispensable. In other words, a device, which has sufficiently high gain in the millimeter-wave region, must be developed for this new age.

For this purpose, p high electron-mobility transistors (p-HEMT's) and InP-based HEMT's have been investigated for several years. However, these devices have a recessed gate structure to reduce parasitic resistance. Consequently, only one type of FET can be fabricated on a wafer, while integrating several different types would be attractive for highly functional integration of MMIC's. In this paper, we will report the simultaneous fabrication of a 0.1-μm class symmetric LDD (lightly doped drain) heterostructure MESFET (H-MESFET) and a new structure, an asymmetric double LDD (D-LDD) H-MESFET, on the same wafer. For this purpose, we will propose a new model to clear the tradeoff relation between gate–drain breakdown voltage and the parasitic resistance.

According to this model, an asymmetric D-LDD H-MESFET with both high gain and high breakdown voltage, and a symmetric LDD H-MESFET with high current gain cutoff frequency (f_T) are successfully fabricated.

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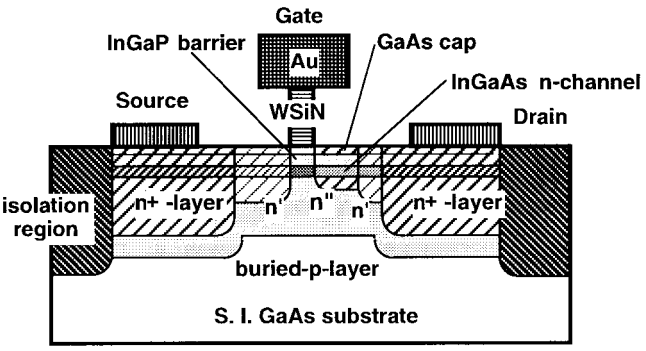


Fig. 1. Schematic cross-sectional view of a D-LDD H-MESFET. The difference from an ordinal LDD MESFET is the addition of n″-implantation between the gate metal and drain-side n′-layer.

II. Device Structure

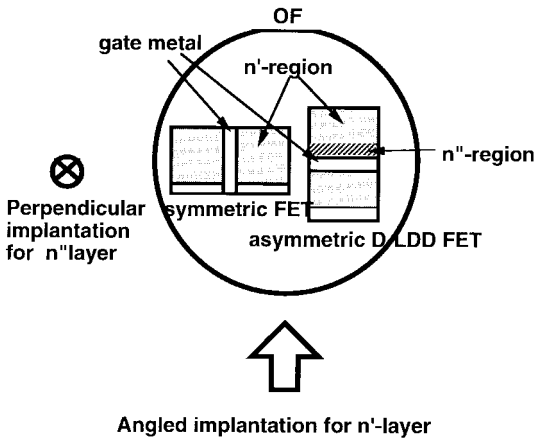
The new structure D-LDD H-MESFET is shown in Fig. 1. It has an i-InGaP barrier layer to improve breakdown voltage [1], [2] and an n-InGaAs channel layer. InGaP is a very promising material for the barrier layer because it has no donor complex (DX) center, but it is difficult to form highly doped n-InGaP. Hence, it is also difficult to attain a sufficiently high sheet carrier in the n-InGaP/GaAs or n-InGaP/InGaAs systems. On the other hand, with i-InGaP/n-InGaAs, it is possible to obtain high sheet carrier [3], [4].

An FET with the D-LDD structure has two lightly doped regions and one heavily doped region only on the drain side, although there is one lightly doped region and one heavily doped region on the source side. The lightly doped region close to the gate is called the n″-layer, and the other lightly doped layer is called the n′-layer. The n″ implantation dose should be less than the n′-layer dose so as not to degrade the gate–drain breakdown voltage $(V_{\rm bgd})$. We used an n″ implantation dose ranging from 1/10 to 1/4 of the n′ implantation dose.

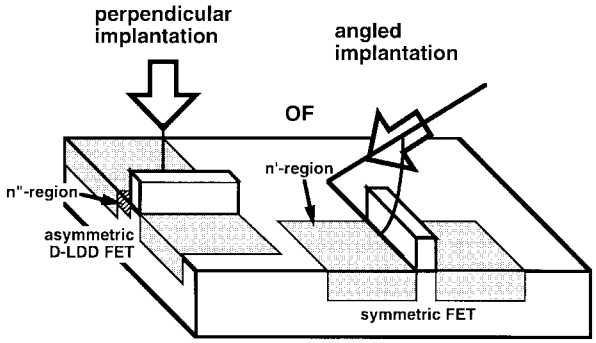
III. Fabrication Process

The integration of D-LDD H-MESFET's and LDD H-MESFET's is easily achieved by changing the n′ ion-implantation tilt angle [5], [6], as shown in Fig. 2.

The gate orientations of a symmetric FET and an asymmetric FET are different, as shown in Fig. 2(a). An n′ ion-implantation is achieved at a tilted angle from the inverse of the orientation flat (OF). The region of shadow of gate metal is not implanted, as shown in Fig. 2(b). After tilted n′-implantation, the n″-layer is implanted perpendicularly to the wafer surface. Thus, the region with no n′-implantation is



(a)



(b)

Fig. 2. Simultaneous fabrication of an asymmetric D-LDD H-MESFET and a symmetric LDD H-MESFET on the same wafer. (a) Gate orientation of both types of FET in a wafer. (b) The relation between gate orientation and ion-implantation tilt-angle.

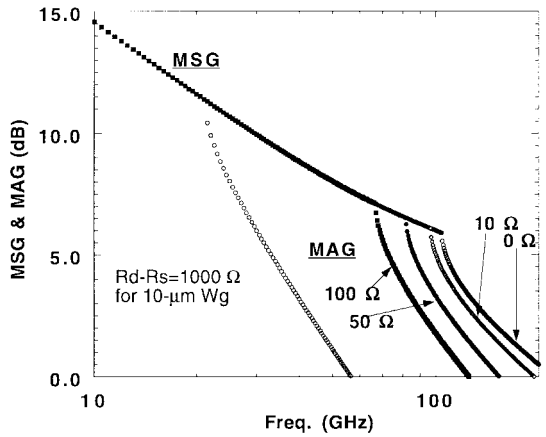


Fig. 3. Role of R_d on maximum stable gain (MSG) and maximum available gain (MAG) frequency characteristics (calculated).

implanted by n″-implantation. This procedure does not affect a symmetric FET's structure. Consequently, symmetric and asymmetric FET's can successfully be fabricated simultaneously on the same wafer.

IV. The Role of R_d on Gain

The simple asymmetric structure reported in [2] and [3] has many advantages for other devices, but it has one problem: drain resistance (R_d) can easily be affected by deviations in gate etching processing because there is a high resistive region with no implantation on the drain side, as shown in Fig. 1. The D-LDD structure is proposed to overcome this drain resistance variation. R_d degrades gain at high frequency (shown in Fig. 3), which is the calculated result. This figure shows that R_d–R_s less than 100 Ω for a 10-μm W_g H-MESFET is necessary for millimeter-wave operation.

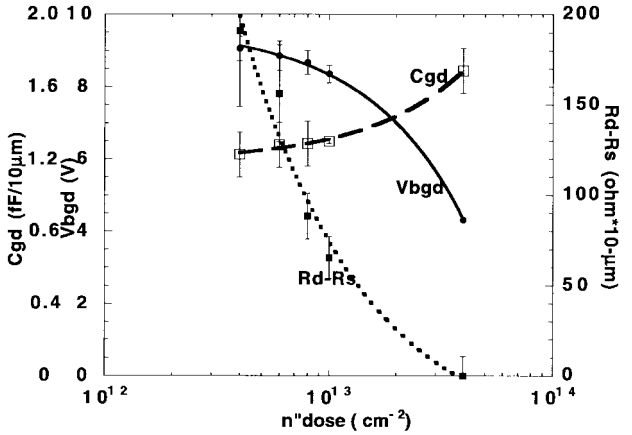


Fig. 4. Dependence of the gate–drain breakdown voltage R_d and $C_{\rm gd}$ on n″-layer dose.

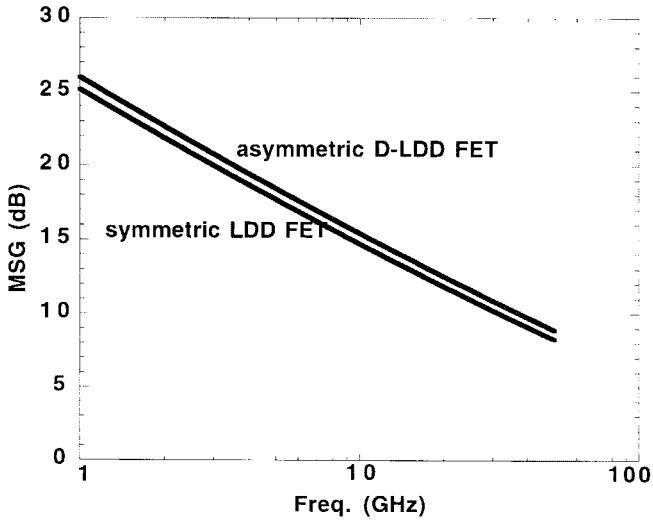


Fig. 5. MSG frequency characteristics of an asymmetric D-LDD H-MESFET and a symmetric LDD H-MESFET on the same wafer.

V. The Results of Device Characteristics

One probable problem caused by n″-implantation is the decrease in gate breakdown voltage. The tradeoff relations between $V_{\rm bgd}$ (gate–drain breakdown voltage) and R_d are shown in Fig. 4 as a function of the n″ ion-implantation dose. Both $V_{\rm bgd}$ and $R_d - R_s$ reduce with increasing n″ dose. $R_d - R_s$ becomes 0 Ω at 4×10^{13} cm^{-2}, because n′-dose is 4×10^{13} cm^{-2} and the FET becomes symmetric at this dose. Fig. 4 shows that a $V_{\rm bgd}$ reduction of only 0.5 V allows a 100-Ω R_d reduction in a 10-μm W_g H-MESFET. Thus, 1×10^{13} cm^{-2} n″ implantation is effective in R_d reduction with the tradeoff that $V_{\rm bgd}$ only decreases by 0.5 V. Another likely problem is the increase in the $C_{\rm gd}$. Fig. 4 is the $C_{\rm gd}$ dependence on n″-implantation dose.

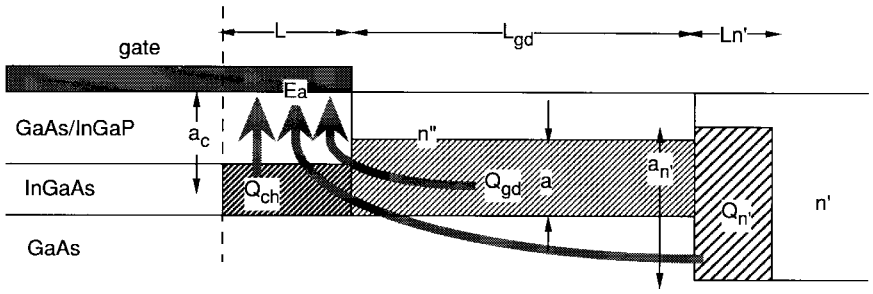


Fig. 6. Detailed cross-sectional view of D-LDD H-MESFET in the gate–drain. Effective width to which electric field lines are terminated in the gate metallization L, distance between gate and drain side n′-layer $L_{\rm gd}$, depleted width by applied drain bias in the n′-layer $L_{\rm n'}$, avalanche breakdown voltage E_a, channel depth ac, n″-layer thickness a, n′-layer thickness $a_{\rm n'}$, total charge in the channel region with L width $Q_{\rm ch}$, total charge in the n″-region $Q_{\rm gd}$, and total charges in the depleted region depleted by gate-drain bias $Q_{\rm n'}$.

The doses of n″-implantation are 4×10^{12}, 6×10^{12}, 8×10^{12}, and 1×10^{13} cm^{-2}. The $C_{\rm gd}$ increase under these conditions is only 0.1–0.2 fF/10 μm.

A 0.10-μm D-LDD H-MESFET with n″-implantation of 1×10^{13} cm^{-2} exhibited high MSG, which is not inferior to a symmetric LDD H-MESFET, as shown in Fig. 5. The measured MAG at 50 GHz and f_T was as high as 8.9 dB and 66.5 GHz. The symmetric H-MESFET exhibits 8.2 dB and 72.1 GHz on the same wafer.

VI. Discussion of $V_{\rm bgd}$ and R_d Tradeoff Relations

In this section, a simple analytical model for predicting gate–drain breakdown voltages is presented, which will be checked by comparing it with experimental results. The method for $V_{\rm bgd}$ prediction is based on Wemple's theory [9] and is modified to apply it to an ion-implanted MESFET. For simplicity, it contains some assumptions as follows.

1) Any accumulation-depletion domains are ignored.
2) The electric field between gate and drain is assumed to be approximately laterally one-dimensional. Only under gate metallization, the electric field is vertically one-dimensional.
3) There is a surface depletion region between gate–drain, and its depth is not affected by drain voltages.
4) The effective width of the electric-field termination region in the gate metallization is assumed to be L.

The cross-sectional view of D-LDD H-MESFET's gate–drain region is shown in Fig. 6. In this figure, the distance between gate metal edge and n′-layer is assigned to $L_{\rm gd}$, the actual distance is 0.2 μm, and the width of depleted n′-layer by drain bias is shown as $L_{\rm n'}$. $Q_{\rm n'}$ is the charge in the depletion region in n′-layer. $Q_{\rm gd}$ and $Q_{\rm ch}$ are the charges in the n″-region and channel region with L length, respectively. E_a is the threshold voltage for breakdown.

Using the notation shown in Fig. 6, $V_{\rm bgd}$ is written as the following expression from Gauss theorem:

$$V_{\rm bgd} = \frac{(L_{\rm gd} + L_{\rm n'}/2) \times Q_{\rm n'}}{\varepsilon_s \times \varepsilon_0 \times a_{\rm n'}} + \frac{(L_{\rm gd}/2) \times Q_{\rm gd}}{\varepsilon_s \times \varepsilon_0 \times a} - V_{\rm th} \quad (1)$$

$$Q_{\rm ch} + Q_{\rm gd} + Q_{\rm n'} = \varepsilon_s \times \varepsilon_0 \times E_a \times L \quad (2)$$

$$Q_{\rm ch} = \frac{\varepsilon_s \times \varepsilon_0 \times L \times V_p}{a_c} \quad (3)$$

$$Q_{\rm gd} = \frac{L_{\rm gd}}{\mu \times R_{\rm sh\_n''}} \quad (4)$$

where $V_{\rm th}$ is the threshold voltage, V_p is the pinchoff voltage, μ is the mobility of the region between gate edge and drain side n′-region, $R_{\rm sh\_n''}$ is the sheet resistance of n″-region, $a, a_{\rm n'}$ are the undepleted thickness of n″-region and n′-region, respectively, a_c is the average depth of the channel layer, ε_s is the dielectric constant, and ε_0 is the vacuum permittivity.

By combining (1)–(4), the following $V_{\rm bgd}$ expression was obtained:

$$V_{\rm bgd} = L \times \left(\frac{L_{\rm gd}}{a_{\rm n'}}\right) \times \left(E_a - \frac{V_p}{a_c}\right) - \frac{L_{\rm gd}^2}{(2\varepsilon_0 \times \varepsilon_S \times \mu)} \times \left(\frac{(2/a_{\rm n'} - 1/a)}{R_{\rm sh\_n''}}\right) - V_{\rm th}. \quad (5)$$

When (5) was extracted from (1)–(4), the following approximation (6) is used:

$$L_{\rm gd} + \frac{L_{\rm n'}}{2} \approx L_{\rm gd}. \quad (6)$$

Simplifying (5), the following new expressions were obtained:

$$V_{\rm bgd} = \alpha - \beta \times V_p - \gamma \times \left(\frac{1}{R_{\rm sh\_n''}}\right) \quad (7)$$

where

$$\alpha = \frac{L \times L_{\rm gd} \times E_a}{a_{\rm n'}} - V_{bi} \quad (8)$$

$$\beta = \frac{L \times L_{\rm gd}}{a_c \times a_{\rm n'}} - 1 \quad (9)$$

$$\gamma = \frac{L_{\rm gd}^2}{2 \times \mu \times \varepsilon_0 \times \varepsilon_s}\left(\frac{2}{a_{\rm n'}} - \frac{1}{a}\right). \quad (10)$$

The important point of (7) is that the $V_{\rm bgd}$ expression contains three terms, and the first term is constant, which determines the upper limit of breakdown voltage, the second term is proportional to V_p, and the third term is inversely proportional to $R_{\rm sh\_n''}$. Thus, the relation between $R_{\rm sh\_n''}$ and $V_{\rm bgd}$ is linear. This can be checked by the above-mentioned experiment.

Fig. 7 shows $R_{\rm sh\_n''}$ dependence on n″-dose. An Si ion was implanted into an metal–organic–chemical vapor deposition-grown (MOCVD) InGaP/InGaAs/GaAs substrate. Ion-implantation energy is 40 kV and amount of n″-dose is from 2.0×10^{12} cm^{-2} to 5.0×10^{13} cm^{-2}. To simulate the FET structure, Be ions are also implanted. Ion-implantation

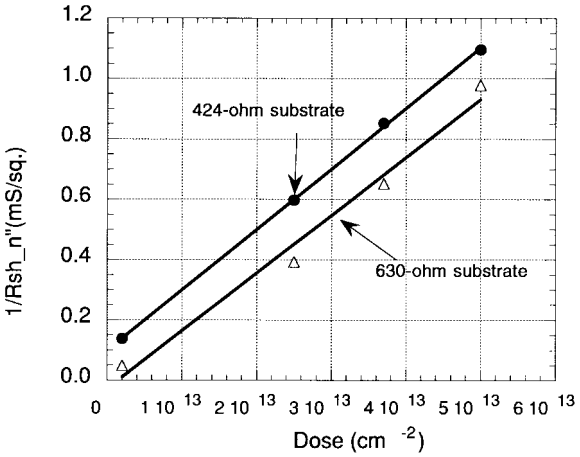


Fig. 7. $R_{\mathrm{sh\_n''}}$ dependence on $\mathrm{n''}$-dose. $\mathrm{n''}$ ion is implanted to InGaP/InGaAs/GaAs substrate with 40 KV implantation energy. Buried p-layer is also implanted. Implantation energy is 50 KV, and dose amount is 2×10^{12} cm^{-2}.

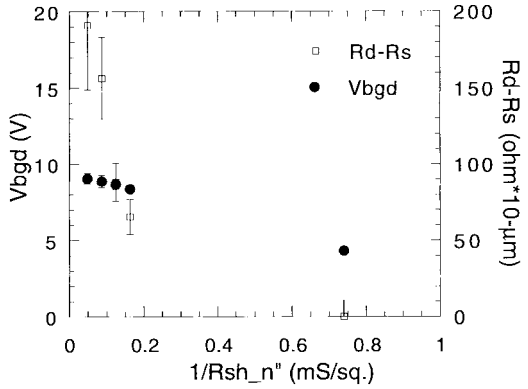


Fig. 8. $R_{\mathrm{sh\_n''}}$, and V_{bgd}, R_d-R_s relation.

energy is 50 KV and the amount of the Be-dose is 2.0×10^{12} cm^{-2}. Resistance of as-grown substrates are 424 Ω^2 and 630 Ω^2. Two lines in Fig. 6 are corresponding to two substrates which are different in as-grown resistance. The obtained conductance is proportional to $\mathrm{n''}$-dose in wide Si-dose. This means that the activation efficiency is constant and the activated carrier is proportional to Si-dose. Using this result, we can estimate carriers in the $\mathrm{n''}$-region.

Fig. 8 is the relation between V_{bgd}, R_d-R_s, and $1/R_{\mathrm{sh\_n''}}$. The predicted linear relation between V_{bgd} and $1/R_{\mathrm{sh\_n''}}$ from (7) is observed, and the slope of the V_{bgd} versus the $1/R_{\mathrm{sh\_n''}}$ line is reasonable for the value calculated from (10). Additionally, a small amount of $\mathrm{n''}$-dose (e.g., of the order of 1×10^{13} cm^{-2}) is effective in R_d-R_s reduction with little V_{bgd} deterioration.

The method for V_{bgd} prediction discussed in this section is general enough, and can be applied to various types of implanted MESFET's.

VII. A One-Stage Amplifier Performance

As a benchmark for high-frequency operation, a one-stage amplifier MMIC of symmetric H-MESFET's was fabricated.

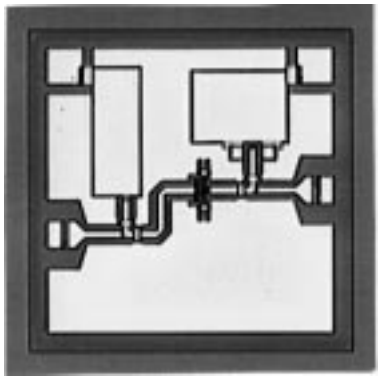


Fig. 9. A fabricated one-stage amplifier MMIC.

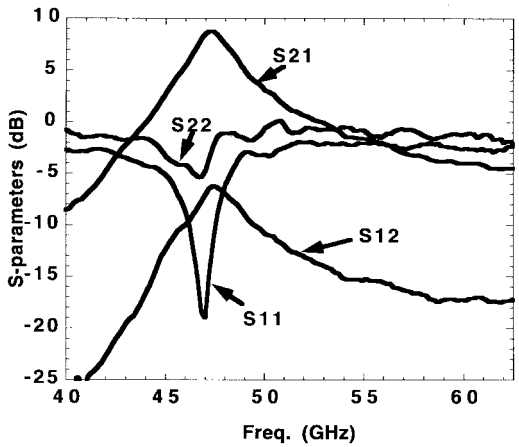


Fig. 10. Measured S-parameters of the one-stage amplifier.

The microphotograph of an MMIC chip is shown in Fig. 9. Fig. 10 shows its measured S-parameters. The maximum measured $S21$ was 8.8 dB at 47.3 GHz. Additionally, all eight measured circuits typically exhibited 7.7 dB $S21$ at 46.7–49.9 GHz. This high performance is superior to any reported for GaAs MMIC's [7], [8] and implies that this technology is most promising for MMIC applications.

VIII. Conclusion

A D-LDD structure for an asymmetric high-power H-MESFET was proposed to stabilize reduced R_d with minimizing V_b deterioration. This FET has been fabricated only by changing ion-implantation tilt angle and gate orientation. By optimizing the $\mathrm{n''}$-layer condition, a D-LDD H-MESFET exhibits over an 8-V breakdown voltage between the gate–drain and a high MSG of 8.9 dB at 50 GHz. Simultaneously, a symmetric LDD H-MESFET has also been fabricated with higher f_T of 72 GHz on a same wafer. To obtain these results, we made a new model for predicting V_{bgd} from $\mathrm{n'}$- and $\mathrm{n''}$-layers sheet resistance, and it was confirmed successfully. This model can be applied to various types of ion-implanted MESFET's.

An one-stage amplifier attained 8.8-dB gain at 47.3 GHz. This high performance shows the possibilities of this device in millimeter-wave applications.

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